5th IEEE Global Conference on Signal & Information Processing

November 14 - 16, 2017, Montreal, Canada

http://www.ieeeglobalsip.org/

Symposium on Signal Processing for Accelerating Deep Learning

Call for Papers

General Co-Chairs:
C.-C. Jay Kuo, University of Southern California
Xiangyang Ji, Tsinghua University

Technical Co-Chairs:
Qixiang Ye, University of Chinese Academy of Science
Yu Wang, Tsinghua University

Deep learning is the hottest topic in AI related research community in last decade, despite DL receive excellent performance in many AI tasks like image classification and nature language processing, its power consumption with GPU platform is too high and limited its usage in energy-sensitive application. On the other hand, recently designed deep networks tend to have more stacked layers, for example, the ResNet, which won the champion in the famous Imagenet Large Scale Image Recognition challenge, have more than 100 network layers and 1 million parameters. The goal of the symposium is to bridge the gap between signal process and deep learning, since a thorough understanding of the parallelism in deep learning algorithms and design limitation of hardware is the key to a successful combined research. The Symposium on Signal Processing for Accelerating Deep Learning will explore the connection between information theory and deep learning, especially will focus on the techniques that will accelerate the deep learning methods in real world applications. This symposium aims to inspire new theoretical methods and new special hardware design for deep learning acceleration. The symposium will be a public forum for researchers to present their most recent works and discuss the future directions, and more importantly, to inspire new idea and promote the theoretical research in deep learning. Technical paper submissions are solicited in the interest topics, which may include, but are not limited to:

- Information theory and deep learning
- Deep learning, a signal processing perspective
- Deep network compression
- Efficient embedded programing for deep learning applications
- Optimization techniques in deep learning
- Sparsity in deep learning
- Accelerating recurrent network
- Scalability issues in deep learning
- GPU/DSP/FPGA/ASIC designs for deep learning
- Special hardware design for deep learning
- High performance hardware for machine leaning
- Digital signal processing for deep learning
- Low rank approximation of deep network
- Hardware architectures for deep learning in the mobile
- Real-time methods and applications of deep learning for smart robot
- Deep learning performance analysis in embed system
- Deep learning in array signal processing

Paper Submission: Prospective authors are invited to submit full-length papers (up to 4 pages for technical content including figures and possible references, and with one additional optional 5th page containing only references) or extended abstracts (up to 2 pages), for paper-less industry presentations and Ongoing Work presentations) via the GlobalSIP 2017 conference website. Manuscripts should be original (not submitted/published anywhere else) and written in accordance with the standard IEEE double-column paper template. Accepted full-length papers will be indexed on IEEE Xplore. Accepted abstracts will not be indexed in IEEE Xplore, however the abstracts and/or the presentations will be included in the IEEE SPS SigPort. Accepted papers and abstracts will be scheduled in lecture and poster sessions.

Important Dates:

- **May 15, 2017**: Paper submission due
- **June 30, 2017**: Notification of Acceptance
- **July 22, 2017**: Camera-ready papers due

For inquiries please contact: Xiangyang Ji (xyji@tsinghua.edu.cn), Qixiang Ye (qxye@ucas.ac.cn), Yu Wang(yu-wang@tsinghua.edu.cn).